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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,854	12/14/2001	Tatsuo Shiozawa	217359US2S	1814
22850	7590	12/27/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			PERILLA, JASON M	
			ART UNIT	PAPER NUMBER
			2638	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/014,854

Applicant(s)

SHIOZAWA ET AL.

Examiner

Jason M. Perilla

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-8,11-15 and 18-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,6-8,13-15 and 20 is/are rejected.
- 7) ☒ Claim(s) 4,5,11-12 and 18-19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1, 4-8, 11-15, and 18-20 are pending in the instant application.

Response to Arguments/Amendments

2. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. New art rejections are set forth below in view of Takano (US 5668840).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 6-8, 13-15, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (AAPA; figs. 5-7; Specification pgs. 1-8) in view of Raphaeli et al (US 2003/0103521; hereafter "Raphaeli" – previously cited), and in further view of Takano (US 5668840)

Regarding claim 1, the AAPA discloses according to figure 7, a radio communication control device comprising: a demodulation unit (13), coupled to an output end of the demodulation unit, configured to demodulate a received signal; a detection circuit (17) configured to detect final data contained in a received data stream supplied from the demodulation unit, said detection circuit outputting a final data notification signal when detecting the final data; and a standby period timer (18) configured to set a standby period in accordance with the final data notification signal

output from said detection circuit (pg. 4, line 25 – pg. 5, line 20). According to the AAPA, the detection circuit or frame receiving unit is able to detect the final data, and, afterwards, the standby period is started (pg. 5, lines 17-20). Although the AAPA does not explicitly disclose the detection circuit being directly coupled to and further configured to output a final data notification signal, *it is disclosed that the counting of the standby period is started when the detection circuit receives (detects) the final data.* Therefore, it is inherent *or at least obvious* that the detection circuit of the AAPA as illustrated in figure 7 and disclosed in the body of the specification (pg. 4, line 25 – pg. 5, line 20) will output at least a start signal which will start the timer or, equivalently, a final data notification signal. Therefore, it is obvious that the standby timer is “coupled” to an output of the detection circuit in some form because the coupling is necessary for the start timer to start counting as disclosed according to the final data notification signal.

Further, the AAPA discloses that the radio data is in conformity with the IEEE 802.11 standard (pg. 2, lines 15-20). The AAPA does not explicitly disclose that the received data includes a data section containing a plurality of symbols and a symbol length indicating section indicating the number of symbols in the data section. However, Raphaeli teaches the format of an IEEE 802.11 frame (para. 265) having a data section or payload (para. 269) and a symbol length field or payload length field (para. 292). Therefore, with reference to the disclosure of Raphaeli regarding the nature of an IEEE 802.11 data frame, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the received data

stream of the AAPA radio device would contain a data and a data length portion because it is the standard frame type utilized in IEEE 802.11 communications.

The AAPA in view of Raphaeli do not disclose that the detection circuit includes an arithmetic operation circuit configured to calculate the number of symbols from the symbol length included in the received data stream; a register configured to hold the number of symbols supplied from said arithmetic operation circuit; a counter configured to count the number of symbols included in the received data stream; and a comparator configured to compare the number of symbols counted by the counter and the number of symbols held by the register with each other, said comparator further configured to output the final data notification signal when these numbers coincide with each other. However, Takano teaches a specific and exemplary implementation of a detection circuit comprising: an arithmetic operation (fig. 3, ref. 7) circuit configured to calculate the number of symbols from the symbol length included in the received data stream; a register (fig. 3, ref. 7) configured to hold the number of symbols supplied from said arithmetic operation circuit; a counter (fig. 3, ref. 6) configured to count the number of symbols included in the received data stream; and a comparator (fig. 3, ref. 8) configured to compare the number of symbols counted by the counter and the number of symbols held by the register with each other, said comparator further configured to output the final data notification signal when these numbers coincide with each other (col. 2, line 55 – col. 3, line 11). The frame length generator (arithmetic operation circuit) performs both the functions of calculating the number of symbols from the symbol length included in the received data stream (fig. 3, ref. 3; col. 2, line2 56-62) and

holding (register) the number of symbols from the symbol length as input to the comparator. The output of the comparator is a final data notification signal. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the detection circuit implementation as taught by Takano in the device of the AAPA in view of Raphaeli because it is a simple and effective method to determine the end of data being received.

Regarding claim 6, the AAPA in view of Raphaeli and in further view of Takano disclose the limitations of claim 1 as applied above. Further, the AAPA discloses according to figure 7, a buffer circuit (15) connected to an output terminal of the detection circuit, and configured to hold symbols outputted from the detection circuit; a Viterbi decoder (16) connected to an output terminal of the buffer circuit, and configured to decode the symbols outputted from the detection circuit, to reproduce a frame; and a frame receiver unit (17) configured to receive the frame outputted from the Viterbi decoder.

Regarding claim 7, the AAPA in view of Raphaeli and in further view of Takano disclose the limitations according to claim 1 above. Further, the AAPA discloses by figure 7 a transmitter unit (20) connected to the standby period timer (18), and configured to transmit a frame in accordance with an output signal of the standby period timer as illustrated (pg. 1, lines 19-26).

Regarding claim 8, the AAPA in view of Raphaeli and in further view of Takano disclose the limitations of the claim as applied to claim 1 above.

Regarding claim 13, the AAPA in view of Raphaeli and in further view of Takano disclose the limitations of claim 8 as applied above. Further, the AAPA discloses according to figure 7, a buffer circuit (15) connected to an output terminal of the detection circuit, and configured to hold symbols outputted from the detection circuit; a Viterbi decoder (16) connected to an output terminal of the buffer circuit, and configured to decode the symbols outputted from the detection circuit, to reproduce a frame; and a frame receiver unit (17) configured to receive the frame outputted from the Viterbi decoder.

Regarding claim 14, the AAPA in view of Raphaeli and in further view of Takano disclose the limitations of claim 8 as applied above. Further, the AAPA discloses by figure 7 a transmitter unit (20) connected to the standby period timer (18), and configured to transmit a frame in accordance with an output signal of the standby period timer as illustrated (pg. 1, lines 19-26).

Regarding claim 15, the AAPA in view of Raphaeli and in further view of Takano disclose the limitations of the claim as applied to claims 8 and 14 above. That is, the AAPA in view of Raphaeli and in further view of Takano disclose the demodulation unit, detection circuit, and standby period timer wherein a transmission is started after the standby period timer elapses (AAPA; pg. 1, lines 19-26) as applied to claims 8 and 14 above.

Regarding claim 20, the AAPA in view of Raphaeli and in further view of Takano disclose the limitations of claim 15 as applied above. Further, the AAPA discloses according to figure 7, a buffer circuit (15) connected to an output terminal of the

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detection circuit, and configured to hold symbols outputted from the detection circuit; a Viterbi decoder (16) connected to an output terminal of the buffer circuit, and configured to decode the symbols outputted from the detection circuit, to reproduce a frame; and a frame receiver unit (17) configured to receive the frame outputted from the Viterbi decoder.

Allowable Subject Matter

5. Claims 4-5, 11-12, and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The Applicant is requested to contact the Examiner before filing a response to discuss allowable subject matter in the application. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jason M. Perilla
September 2, 2005



KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER

jmp